Telecommunications
Communications Technologies

Quadrature Phase Shift Keying (QPSK/DQPSK)

Courseware Sample

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Safety and Common Symbols

The following safety and common symbols may be used in this manual and on the equipment:

Symbol	Description
⚠ DANGER	**DANGER** indicates a hazard with a high level of risk which, if not avoided, will result in death or serious injury.
⚠ WARNING	**WARNING** indicates a hazard with a medium level of risk which, if not avoided, could result in death or serious injury.
⚠ CAUTION	**CAUTION** indicates a hazard with a low level of risk which, if not avoided, could result in minor or moderate injury.
CAUTION	**CAUTION** used without the *Caution, risk of danger* sign ⚠, indicates a hazard with a potentially hazardous situation which, if not avoided, may result in property damage.
	Caution, risk of electric shock
	Caution, hot surface
	Caution, risk of danger
	Caution, lifting hazard
	Caution, hand entanglement hazard
	Notice, non-ionizing radiation
	Direct current
	Alternating current
	Both direct and alternating current
	Three-phase alternating current
	Earth (ground) terminal

Safety and Common Symbols

Symbol	Description
	Protective conductor terminal
	Frame or chassis terminal
	Equipotentiality
	On (supply)
	Off (supply)
	Equipment protected throughout by double insulation or reinforced insulation
	In position of a bi-stable push control
	Out position of a bi-stable push control

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Preface

Digital communication offers so many advantages over analog communication that the majority of today's communications systems are digital.

Unlike analog communication systems, digital systems do not require accurate recovery of the transmitted waveform at the receiver end. Instead, the receiver periodically detects which waveform is being transmitted, among a limited number of possible waveforms, and maps the detected waveform back to the data it represents. This allows extremely low error rates, even when the signal has been corrupted by noise.

The digital circuits are often implemented using application specific integrated circuits (ASIC) and field-programmable gate arrays (FPGA). Although this "system-on-a-chip" approach is very effective for commercial and military applications, the resulting systems do not allow access to internal signals and data and are therefore poorly suited for educational use. It is for this reason that we designed the Communications Technologies Training System.

The Communications Technologies Training System, Model 8087, is a state-of-the-art communications training system. Specially designed for hands-on training, it facilitates the study of many different types of digital modulation/demodulation technologies such as PAM, PWM, PPM, PCM, Delta Modulation, ASK, FSK, and BPSK as well as spectrally efficient technologies such as QPSK, QAM, and ADSL. The system also enables the study of direct-sequence and frequency-hopping spread spectrum (DSSS and FHSS), two key technologies used in modern wireless communication systems (CDMA cellular-telephony networks, Global Positioning System, Bluetooth interface for wireless connectivity, etc.) to implement code-division multiple access (CDMA), improve interference rejection, minimize interference with other systems, etc. The system is designed to reflect the standards commonly used in modern communications systems.

Unlike conventional, hardware-based training systems that use a variety of physical modules to implement different technologies and instruments, the Communications Technologies Training System is based on a Reconfigurable Training Module (RTM) and the Communications Technologies (LVCT) software, providing tremendous flexibility at a reduced cost.

Each of the communications technologies to be studied is provided as an application that can be selected from a menu. Once loaded into the LVCT software, the selected application configures the RTM to implement the communications technology, and provides a specially designed user interface for the student.

The LVCT software provides settings for full user control over the operating parameters of each communications technology application. Functional block diagrams for the circuits involved are shown on screen. The digital or analog signals at various points in the circuits can be viewed and analyzed using the virtual instruments included in the software. In addition, some of these signals are made available at physical connectors on the RTM and can be displayed and measured using conventional instruments.

The courseware for the Communications Technologies Training System consists of a series of student manuals covering the different technologies as well as instructor guides that provide the answers to procedure step questions and to

review questions. The Communications Technologies Training System and the accompanying courseware provide a complete study program for these key information-age technologies.

We invite readers of this manual to send us their tips, feedback, and suggestions for improving the book.

Please send these to did@de.festo.com.

The authors and Festo Didactic look forward to your comments.

Acknowledgements

We thank the following people for their participation in the development of the Communications Technologies Training System: Richard Tervo, Ph.D., P.Eng. from the University of New Brunswick, and John Ahern, M.Sc.A. and Marcel Pelletier, Ph.D. from Comlab Telecommunications Inc.

About This Manual

Manual Objective

When you have completed this manual, you will be familiar with the principles of QPSK modulation and demodulation. You will be familiar with the use of differential QPSK (DQPSK) to overcome phase ambiguity and with the use of data scrambling to ensure frequent transitions in the modulated signal. You will also be able to troubleshoot instructor-inserted faults in the QPSK/DQPSK application.

Description

This Student Manual begins with an Introduction presenting important background information. Following this are a number of exercises designed to present the subject matter in convenient instructional segments. In each exercise, principles and concepts are presented first followed by a step-by-step, hands-on procedure to complete the learning process.

Each exercise contains:

- A clearly defined Exercise Objective
- A Discussion Outline listing the main points presented in the Discussion
- A Discussion of the theory involved
- A Procedure Outline listing the main sections in the Procedure
- A step-by-step Procedure in which the student observes and measures the important phenomena, including questions to help in understanding the important principles.
- A Conclusion
- Review Questions

In this manual, all New Terms are defined at the end of the Introduction. In addition, an Index of New Terms is provided at the end of this manual.

Preparation

Before beginning this manual, it is preferable to be familiar with the following topics:

- Pseudo-random binary sequences (PRBSs), also called pseudo-random bit sequences, n-sequences or maximum-length sequences — their time-domain and frequency-domain characteristics.
- Binary phase shift keying (BPSK) — the generation and demodulation of BPSK signals and their time-domain and frequency-domain characteristics.

About This Manual

Safety considerations

Safety symbols that may be used in this manual and on the equipment are listed in the Safety Symbols table at the beginning of the manual.

Safety procedures related to the tasks that you will be asked to perform are indicated in each exercise.

Make sure that you are wearing appropriate protective equipment when performing the tasks. You should never perform a task if you have any reason to think that a manipulation could be dangerous for you or your teammates.

Systems of units

Units are expressed using the International System of Units (SI) followed by units expressed in the U.S. customary system of units (between parentheses).

Conventions Used in This Manual

Special character formats

Colored sidebars contain complementary information that will be of interest to the reader.

New terms are shown in **bold colored characters** the first time they appear.

Important terms are shown in **bold colored characters** the first time they appear.

Notes provide details that should be noted by the reader.

Tips provide information on effectively using the system. These are particularly helpful for inexperienced users.

This symbol refers you to another manual or document.

Software commands and dialog box names are shown in color. "Choose *File* ▶ *Print*" means choose the *Print* command in the *File* menu.

Probe connections

Instrument probe connections to test points are usually presented in tables showing the type of probe to use, the test point (TP) to connect it to, and the signal present at that test point:

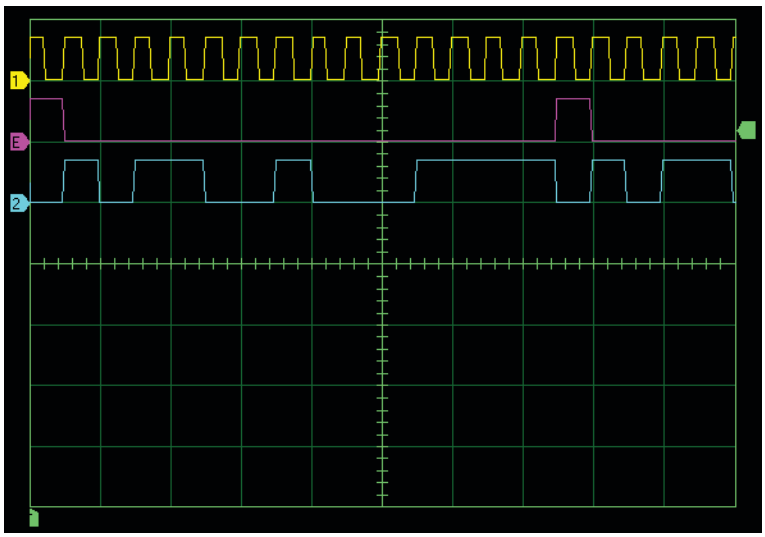
Oscilloscope probe	Connect to	Signal
1	TP1	DATA INPUT
2	TP2	CLOCK INPUT
E	TP3	BSG SYNC. OUTPUT

System and instrument settings

Unless you are instructed to make specific settings, you can use any system and instrument settings that will allow you to observe the phenomena of interest. As a guide, important settings that were used to produce a figure may be shown beside the figure.

Generator Settings:
Bit Rate .....2000 bit/s
n 4

Oscilloscope Settings:
Channel 1.....5 V/div
Channel 2.....5 V/div
Channel E .....5 V/div
Time Base..... 1 ms/div
Trigger: Slope .....Rising
Trigger: Level ..... 1 V
Trigger: Source ..... Ext



List of Equipment Required

The following equipment is required to perform the procedures in this manual:

QTY	DESCRIPTION	MODEL
1	Power Supply	9408
1	Reconfigurable Training Module	9431
1	Data Acquisition Interface	9466
1	Analog/Digital Output Interface	9467
1	LVCT Software	9432-0
1	QPSK / QAM / ADSL Applications	9432-4
1	Cables and Accessories	9483

Additional Equipment

The LVCT software requires a current model computer running Windows® operating system. An Ethernet (100 Mb/s or better) network interface adapter is also required. A dual-output video adapter and two monitors are recommended to allow viewing the diagrams and the virtual instruments simultaneously.

The Communications Technologies Host Computer, Model 9695-A0, meets or exceeds these requirements.

Optional Equipment

You may wish to use a conventional oscilloscope (Model 797-20 or equivalent) and/or spectrum analyzer to observe the signals available at the BNC connectors and test points on the RTM (refer to the RTM Connections tab of the software to identify these outputs).

To the Instructor

You will find in this Instructor Guide all the elements included in the Student Manual together with the answers to all questions, results of measurements, graphs, explanations, suggestions, and, in some cases, instructions to help you guide the students through their learning process. All the information that applies to you is placed between markers and appears in red.

Accuracy of measurements

The numerical results of the hands-on exercises may differ from one student to another. For this reason, the results and answers given in this manual should be considered as a guide. Students who correctly performed the exercises should expect to demonstrate the principles involved and make observations and measurements similar to those given as answers.

Sample Exercise
Extracted from
the Student Manual
and the Instructor Guide

QPSK Modulation

EXERCISE OBJECTIVE

When you have completed this exercise, you will be familiar with QPSK modulation, with the characteristics of QPSK signals and with the QPSK signal constellation. You will also be familiar with the LVCT software and the use of the virtual instruments.

DISCUSSION OUTLINE

The Discussion of this exercise covers the following points:

- The QPSK waveform
- QPSK constellations
- A typical QPSK modulator
- Symbol rate and bandwidth

DISCUSSION

The QPSK waveform

* Filters are usually used near the output of a QPSK modulator in order to restrict the bandwidth. This results in amplitude variations in the QPSK signal. Although these amplitude variations facilitate timing recovery in the demodulator, they do not convey data. Only the phase of the waveform conveys the data.

With quadrature phase shift keying modulation (also called quaternary PSK, quadriphase PSK or 4-PSK), a sinusoidal waveform is varied in phase while keeping the amplitude* and frequency constant. The term *quadrature* indicates that there are four possible phases.

Equation (3) shows the general expression for a QPSK waveform.

$$s_i(t) = A\cos\left[\omega_c t + \varphi_0 + \varphi_i(t)\right] \quad (3)$$

where
- s_i is the PSK signal waveform for phase *i*
- t is time
- A is the peak amplitude
- ω_c is the carrier frequency in radians/s ($\omega_c = 2\pi f_c$)
- φ_0 is the reference phase angle
- φ_i is phase *i*
- i ranges from 1 to 4

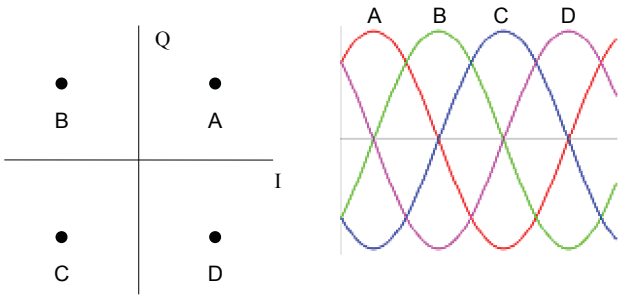
The instantaneous phase has discrete values equal to $\varphi_0 + \frac{2\pi i}{4}$, where *i* = 1, 2, 3, or 4.

QPSK constellations

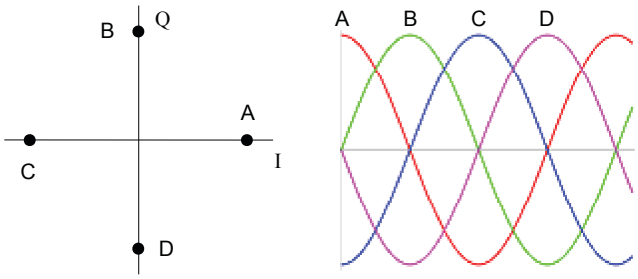
The ideal PSK constellation has *M* equidistant phase states and constant amplitude, resulting in a circular symmetry. With QPSK, therefore, *M* = 4 and the phases are separated by 90°, as shown in Figure 4.

Figure 4 shows two common representations of the QPSK constellation. The constellation points are arbitrarily labeled A, B, C and D, each of which represents one of the four possible dibits 00, 01, 10, and 11. The mapping between the dibits and the constellation points depends on the modulator circuit.

Beside each constellation in Figure 4 is a plot showing all four phases (modulation symbols) as sinusoids. In each of these representations, the four phases are spaced 90° (π/2 radians) apart. The only difference between these representations is the choice of the reference phase angle (φ_0 in Equation (3)).



a) QPSK (φ = π/4, 3π/4, 5π/4, 7π/4)



b) QPSK (φ = 0, π/2, π, 3π/2)

Figure 4. QPSK constellation and waveforms.

A typical QPSK modulator

A QPSK signal can be generated by independently modulating two carriers in quadrature (cos ωt and sin ωt), as shown in Figure 5.

The Serial to Parallel Converter groups the incoming data into dibits (groups of two consecutive bits). Each time two bits have been clocked serially into its buffer, the Serial to Parallel Converter outputs one dibit in parallel at its two outputs.

One bit of each dibit is sent to the I channel of the modulator; the other bit is sent to the Q channel of the modulator. Each channel of the modulator works independently to processes the stream of bits it receives.

The starting point for grouping bits into dibits is *completely arbitrary*. For educational purposes, the Serial to Parallel Converter in the QPSK application has a **Drop 1 Bit button**. Clicking this button causes the Serial to Parallel Converter to ignore one bit in the data sequence. This changes the grouping of all subsequent data bits into dibits.

The Level Converter in each channel converts the data into a (baseband) bipolar pulse stream that can be applied to one input of the mixer. To restrict the bandwidth of the QPSK signal, a Low-Pass Filter is usually used before the mixer in each channel of the modulator in order to provide the desired spectral shaping. In addition, a bandpass filter (not shown in Figure 5) may be used to filter the QPSK signal before transmission.

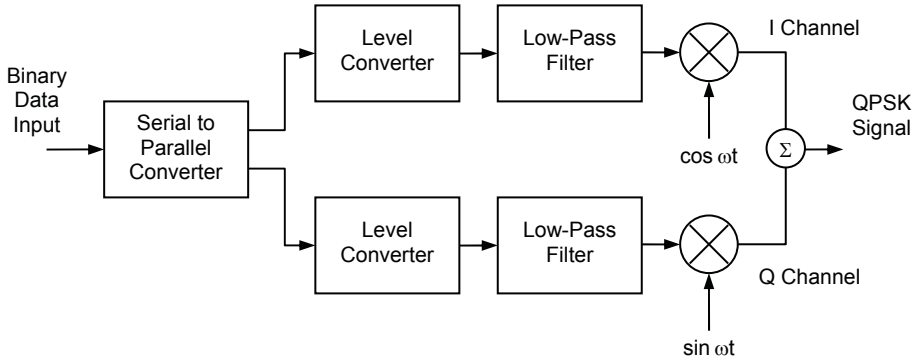


Figure 5. Simplified block diagram of a QPSK modulator.

The I- and Q-channel sinusoidal carriers $\cos \omega t$ and $\sin \omega t$ are in quadrature (90° out of phase). Each mixer performs modulation by multiplying the carrier by the bipolar data signal in order to produce a BPSK signal. The effect of the mixer is to shift the frequency spectrum of the baseband signal up to the frequency of the carrier.

Orthogonal signals can be summed, transmitted in a channel and (theoretically) perfectly separated in the demodulator without any mutual interference.

The two BPSK signals are summed to produce the QPSK signal. Because these two BPSK signals are generated using two carriers in phase quadrature, the BPSK signals are **orthogonal**, and the QPSK demodulator will be able to demodulate them separately.

The output signal of the modulator is a sinusoidal carrier with four possible phases, each of which represents a two-bit symbol. This signal can be represented by Equation (4).

If the levels of the bipolar pulses d_0, d_1, etc. are +1 and -1, the peak amplitude of the waveform represented by Equation (4) is $\sqrt{2}$. The factor $1/\sqrt{2}$ could be included in this equation to normalize the amplitude to unity.

$$s(t) = d_I(t)\cos(\omega t) + d_Q(t)\sin(\omega t) \qquad (4)$$

where
- $s(t)$ is the QPSK signal waveform
- $d_I(t)$ is the I-channel bipolar pulse stream d_0, d_2, d_4 …
- $d_Q(t)$ is the Q-channel bipolar pulse stream d_1, d_3, d_5 …
- ω is the angular frequency

Figure 6 shows the waveforms present in a modulator with no filtering. The bipolar I-channel and Q-channel pulses have levels of +1 and -1. The QPSK signal shown in Figure 6 has discontinuities which increase the bandwidth of the signal. The Low-Pass Filters shown in Figure 5 smooth the discontinuities and decrease the effective bandwidth.

Figure 6 shows all waveforms synchronized in time. In a real system, processing delays will cause successive signals to be slightly offset in time.

Figure 6 shows the dibit 11 mapped to the constellation point in the first quadrant. Other mappings are possible. Such mappings usually use a Gray code to ensure that only one bit changes between adjacent symbols. As a result, QPSK modulators map the dibits 00 and 11 to opposite quadrants.

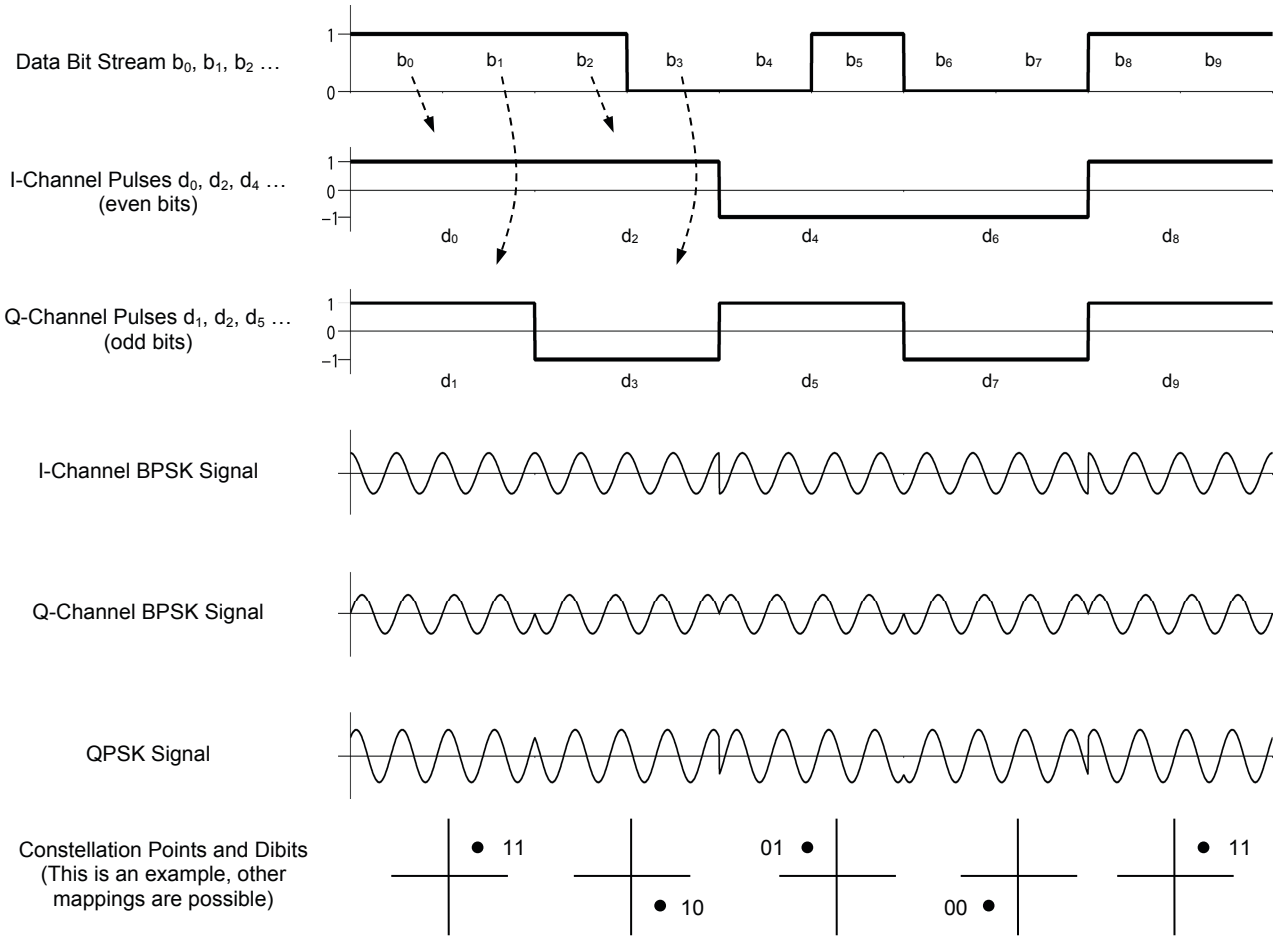


Figure 6. QPSK signal generation from two BPSK signals.

Symbol rate and bandwidth

Because each symbol represents two bits, the rate that the symbols occur in the QPSK signal (the symbol rate) is one half the bit rate. Table 2 compares the symbol rates (and bandwidths) for BPSK and QPSK.

Table 2. Symbol rate and bandwidth for BPSK and QPSK.

Modulation	Bits per symbol	Symbol rate vs. Bit rate	First-nulls bandwidth
BPSK	1	$R_s = R_b$	$2R_b$
QPSK	2	$R_s = \frac{R_b}{2}$	R_b

The bandwidth of a modulated signal depends on the rate of change in the signal (i.e. the symbol rate) and not on the magnitude of each change. For this reason, using QPSK rather than BPSK will reduce by one-half the bandwidth required for a given bit rate. Alternatively, using QPSK can double the bit rate for a given signal bandwidth. This is illustrated in Figure 7, where f_c is the carrier frequency.

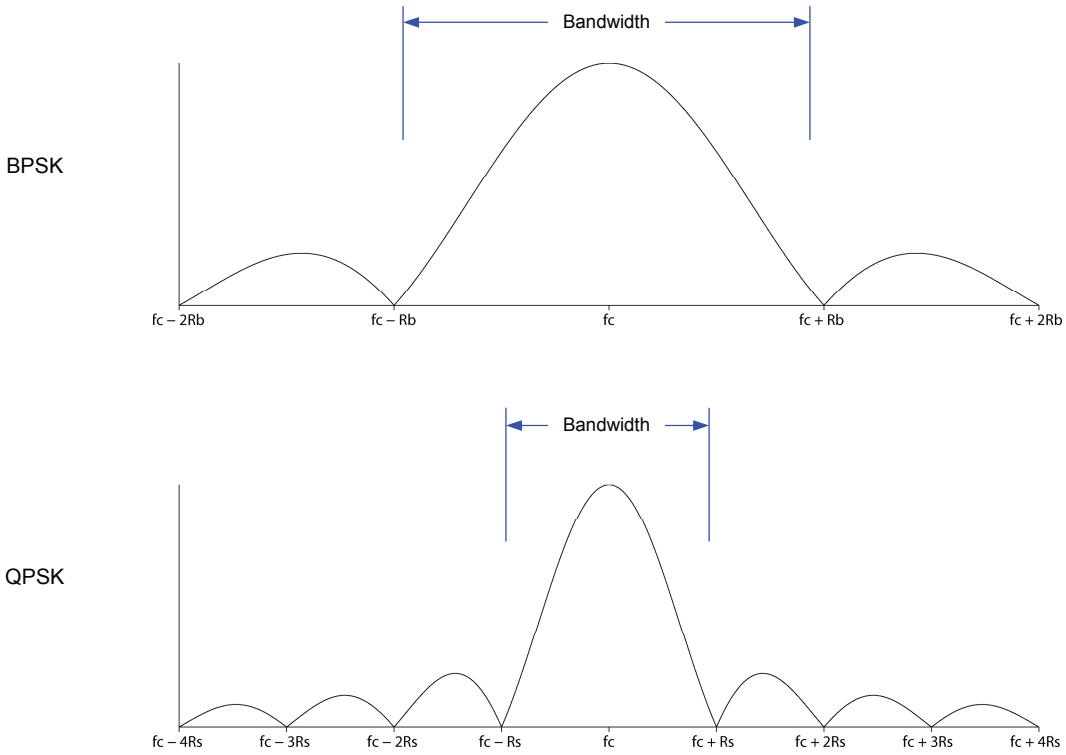


Figure 7. BPSK and QPSK magnitude spectrum (for equal bit rates).

Figure 7 shows that the first-nulls bandwidth of a BPSK signal is $2R_b$ and that of a QPSK signal with the same bit rate is $2R_s = R_b$. Since $R_s = \frac{R_b}{2}$ for QPSK, the bandwidth efficiency of QPSK is twice that of BPSK.

The modulated signal is called a double-sideband suppressed-carrier signal, since its bandwidth is twice that of the baseband signal and there is no isolated signal at the carrier frequency.

PROCEDURE OUTLINE

The Procedure is divided into the following sections:

- Set-up and connections
- Observing binary sequences on the Oscilloscope
- Observing binary sequences on the Spectrum Analyzer
- Using the Logic Analyzer
- The Serial to Parallel Converter
- Level Converter
- The Filters and mixers
- The summer
- Signal constellations

PROCEDURE

Set-up and connections

1. Turn on the RTM Power Supply and the RTM and make sure the RTM power LED is lit.

File ▶ Restore Default Settings *returns all settings to their default values, but does not deactivate activated faults.*

2. Start the LVCT software. In the Application Selection box, choose *QPSK/DQPSK* and click OK. This begins a new session with all settings set to their default values and with all faults deactivated.

   If the software is already running, choose *Exit* in the *File* menu and restart LVCT to begin a new session with all faults deactivated.

3. Make the Default external connections shown on the System Diagram tab of the software. For details of connections to the Reconfigurable Training Module, refer to the RTM Connections tab of the software.

   Click the **Default** button to show the required external connections.

4. As an option, connect a conventional oscilloscope to the BSG CLOCK OUTPUT and the BSG DATA OUTPUT, using BNC T-connectors. Use the BSG SYNC./2 OUTPUT as an external trigger.

   On-line help is accessible from the *Help* menu of the software and the *Help* menu of each instrument.

   You can print out the screen of any instrument by choosing *File* ▶ *Print* in that instrument.

Observing binary sequences on the Oscilloscope

5. Make the following Generator Settings:

   Generation Mode .....Pseudo-Random
   n.....4
   Bit Rate .....2000 bit/s

Settings

This application has tables of settings that allow you to change various software parameters in order to configure the system. Two Settings tables are provided – QPSK Settings and Generator Settings. By default, these tables are located at the right side of the main window and only one of these tables is visible at a time. Two tabs at the bottom allow you to select which table is visible and the name of the visible table is displayed at the top. (Refer to on-line help for more information.)

Settings tables have two columns. The name of each setting is shown in the left column and the current value of each setting is shown in the right column. The column separator can be moved using the mouse, and the entire table can be resized as desired.

Some settings have a drop-down list of possible values. To change this type of setting, click the setting and then click the down arrow to display the drop-down list and select a new value. You can also click the setting and then roll the mouse wheel to change the value or repeatedly double-click the setting to cycle through the available values.

To change an editable numerical setting, simply select or delete the current value in the settings table, type a new value and press Enter or Tab. You can also click the setting and roll the mouse wheel. When fine adjustments are possible, holding down the Ctrl key on the keyboard while rolling the mouse wheel will change the value by small increments.

When you change the value of a numerical setting, the focus remains on that setting until you click elsewhere in the software. To immediately change the setting to another value, you can simply type the new value and press Enter.

6. Click the QPSK Modulator tab in order to display the QPSK Modulator diagram.

Show the Probes bar (click in the toolbar or choose *View* ▶ *Probes Bar*). Connect the Oscilloscope probes as follows:

Oscilloscope probe	Connect to	Signal
1	TP2	CLOCK INPUT
2	TP1	DATA INPUT
E	TP3	BSG (Binary Sequence Generator) SYNC. OUTPUT

To move a probe from the Probes bar to a test point, click the probe, move the mouse until the tip of the probe is over the test point, and click the mouse button to connect the probe.

To move a probe from one test point to another, move the mouse pointer over the probe until the pointer changes into a grasping hand . Then, click the probe and, *without releasing* the mouse button, drag the probe to another test point. Release the mouse button.

7. Show the Oscilloscope (click in the toolbar or choose *Instruments* ▶ *Oscilloscope*). Figure 8 shows an example of settings and what you should observe.

Unless you are instructed to make specific settings, you can use any system and instrument settings that will allow you to observe the phenomena of interest. As a guide, important settings that were used to produce a figure may be shown beside the figure.

Generator Settings:
Generation Mode .....Pseudo-Random
n 4
Bit Rate ..... 2000 bit/s

Oscilloscope Settings:
Channel 1.....5 V/div
Channel 2.....5 V/div
Channel E .....5 V/div
Time Base..... 1 ms/div
Trigger: Slope .....Rising
Trigger: Level..... 1 V
Trigger: Source .....Ext

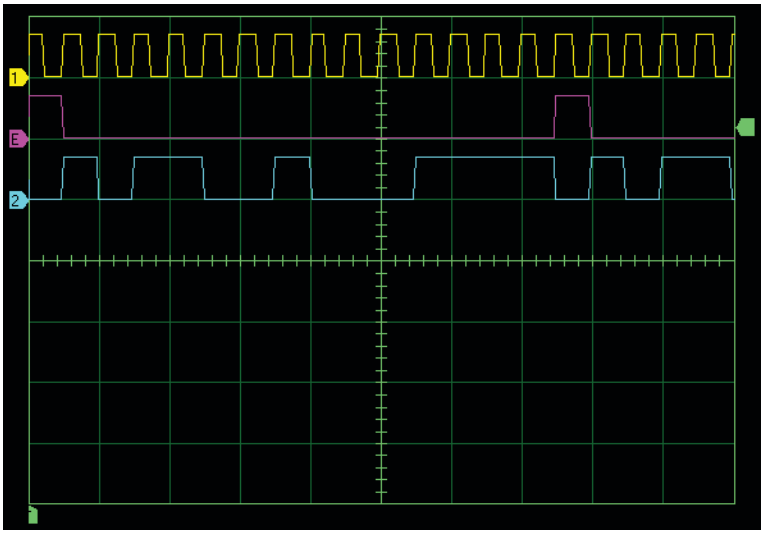


Figure 8. Clock, Sync. and PRBS Data digital (TTL level) signals.

To display the trace of any channel on the Oscilloscope, you must set the Visible setting for that channel to On. (You can trigger the Oscilloscope on a channel even when Visible is set to Off.)

Channel 1 on the Oscilloscope shows the clock signal. Channel E (External) shows the BSG SYNC. signal, which is used as the trigger source for the Oscilloscope. This signal goes high for one clock period at the beginning of each sequence period. Note that the level changes of the pulses in the other signals align with the *rising* edges of the clock signal.

Channel 2 shows a pseudo-random binary sequence (PRBS). With, n = 4 in the Generator Settings, the length $L = 2^4-1 = 15$. Count the number of clock cycles from one sync. pulse to the next to verify that this is the case. Note that the PRBS begins to repeat at the second sync. pulse.

To refresh and freeze the display, click the button in the instrument toolbar. This refreshes the display once and freezes it. You can also press F5 or choose *View* ▶ *Single Refresh*. Click , press F6 or choose *View* ▶ *Continuous Refresh* to resume normal operation.

8. Experiment with the Binary Sequence Generator by changing the value of n and the Bit Rate. Adjust the Time Base on the Oscilloscope as necessary.

In order for the Oscilloscope to trigger properly, the Time Base must be set so that at least one complete period of the Trigger Source signal is displayed on the screen.

Observing binary sequences on the Spectrum Analyzer

9. Minimize the Oscilloscope. Connect the Spectrum Analyzer probe to TP1 (you do not need to disconnect the Oscilloscope probe).

Show the Spectrum Analyzer (click in the toolbar or choose *Instruments* ▶ *Spectrum Analyzer*). Figure 9 shows an example of settings and what you should observe. In the Generator Settings, vary the value of n and the Bit Rate and observe the effect on the spectrum.

To reduce fluctuations in the displayed spectrum, set Averaging to the number of consecutive spectra to be averaged. The higher the setting, the lower the fluctuations, however, the spectrum will take longer to stabilize after a change.

Generator Settings:
Generation Mode ..... Pseudo-Random
n 3
Bit Rate ..... 5000 bit/s

Spectrum Analyzer Settings:
Maximum Input ..... 10 dBV
Scale Type ..... Logarithmic
Scale ..... 10 db/div
Averaging 4
Time Window ..... Square
Frequency Span ..... 2 kHz/div
Reference Frequency 0
Cursors ..... Vertical

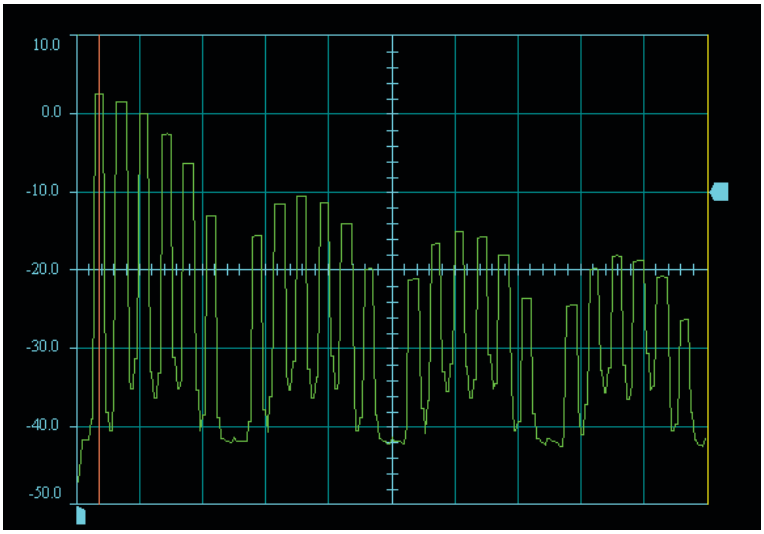


Figure 9. Spectrum of a PRBS.

Use a vertical cursor, as shown in the figure, to determine the approximate frequency of various spectral elements. You can position each cursor by dragging it with the mouse.

Theoretically, the spectral lines have an infinitesimal width. On a spectrum analyzer, however, they appear as bars or peaks. If the spectral lines are very close together, they are not resolved by the Spectrum Analyzer and the spectrum appears to be continuous.

Describe the spectrum of a baseband PRBS.

The spectrum of a PRBS consists of a series of lobes of decreasing magnitude with nulls at multiples of the Bit Rate R_b. This makes the first-null bandwidth equal to the bit rate.

Since the data signal is not truly random but consists of a sequence that repeats every $L = 2^n-1$ bits, the spectrum is not continuous. Instead, it consists of spectral lines spaced at frequencies that are multiples of $\frac{1}{T} = \frac{R_b}{2^n-1}$ where T is the period of the sequence in seconds.

10. In the Generator Settings, set the Generation Mode to User Entry. Enter different binary sequences in the Binary Sequence setting and observe the result using both the Oscilloscope and the Spectrum Analyzer.

When the Generation Mode is set to User Entry, the Binary Sequence Generator generates a repeating binary sequence defined by the Binary

Sequence setting. You can enter up to 32 binary digits (1s and 0s) in this setting. You can include spaces in this setting to make the pattern more legible (the software ignores spaces in this setting).

Using the Logic Analyzer

11. Connect the Logic Analyzer probes as follows:

Logic analyzer probe	Connect to	Signal
C	TP2	CLOCK INPUT
2	TP1	DATA INPUT
1	TP3	BSG SYNC. OUTPUT

Show the Logic Analyzer (click in the toolbar or choose *Instruments* ▶ *Logic Analyzer*). Make the Logic Analyzer settings shown in Figure 10.

Make the following Binary Sequence Generator settings:

Generation Mode .....Pseudo-Random
n 4
Bit Rate .....2000 bit/s

Click in the Logic Analyzer toolbar to record data. Figure 10 shows an example of settings and what you should observe. Compare the signals as displayed on the Logic Analyzer with the same signals as displayed on the Oscilloscope.

Generator Settings:
Generation Mode .....Pseudo-Random
n 4
Bit Rate ..... 2000 bit/s

Logic Analyzer Settings:
Display Width..... 10 ms
Clock Grid .....Falling Edge
Source..... Ch 1
Source Edge .....Rising
Clock Edge ..... Falling
S1 Data.....[ch1]
S2 Data.....[ch2]

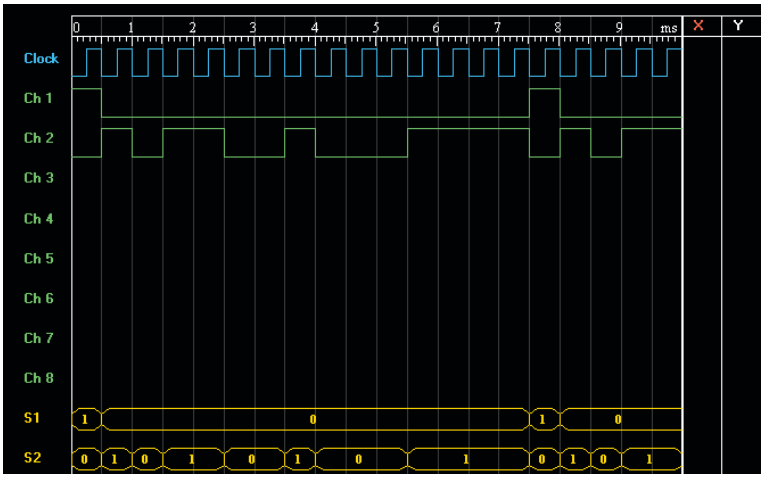


Figure 10. Clock, sync. and data on Logic Analyzer.

Note that the signals displayed on the Oscilloscope and on the Logic Analyzer are very similar. With the Logic Analyzer settings shown in Figure 10, however, the level changes of the pulses in the Sync. signal (Ch 1) and in the Data signal (Ch 2) align with the *falling* edges of the Clock signal.

Logic Analyzer operation

The Logic Analyzer does not display data in real time. Instead, after you click ●, it waits for the trigger and then begins recording data. When its memory is full, it stops recording and displays the recorded data.

The **Source** setting determines which signal is used to trigger the recording and the **Source Edge** setting determines whether the rising edge or the falling edge of this signal triggers the recording.

When recording data, the Logic Analyzer samples each channel *only once per clock period.* The display shows either a high level (1) or a low level (0) in the corresponding trace for each sample taken. The **Clock Edge** setting determines whether the sampling instants correspond to the rising edges or the falling edges of the clock signal. (For this reason, the Logic Analyzer cannot display the precise timing relationship between signals as does the Oscilloscope.)

The following sequence shows how the Logic Analyzer records data:

- The user clicks ● or presses F5 or selects *View* ▶ *Record*.
- The Logic Analyzer waits for the selected Source Edge (Rising or Falling) of the trigger Source signal.
- The Logic Analyzer takes one sample of each channel at each selected Clock Edge (Rising or Falling) until 256 samples of each channel have been recorded. It then updates the display.

The Oscilloscope shows that the transitions in the DATA INPUT signal occur on the *rising* edges of the clock signal. Therefore it is preferable to set Clock Edge to *Falling* as this ensures that the signal will be sampled in the middle of each bit, where the signal voltage is not changing. (Setting Clock Edge to Rising would cause the Logic Analyzer to sample the DATA INPUT signal exactly where the transitions occur, which could result in ambiguous values.)

To observe the output of a functional block that is *falling-edge triggered*, as indicated by the symbol  at the clock input, it is preferable to set Clock Edge to *Rising*.

The Serial to Parallel Converter

12. Make the following Binary Sequence Generator settings:

Generation Mode	User Entry
Binary Sequence	1001 1000 1110 1110
Bit Rate	2000 bit/s

The Serial to Parallel Converter groups the input data stream into dibits and sends the first bit of each dibit to the I Channel of the modulator and the second bit to the Q Channel of the modulator. Since the Serial to Parallel Converter is not synchronized with the data, the grouping into dibits can start at any bit. Because the above Binary Sequence consists of an even number of bits, there are two possible conditions: A) the grouping starts with the *first* bit of the sequence shown above, giving dibits 10, 01, 10, etc. or B) the grouping starts with the *second* bit of the sequence shown above, giving dibits 00, 11, 00, etc.

If the grouping starts with any other bit, the result is equivalent to condition A or B, since the sequence repeats indefinitely.

The first row of Table 3 shows the data bits from this Binary Sequence. After 16 bits, the sequence begins to repeat. A and B in the table represent two ways the data bits can be grouped into dibits. Complete the two **Dibit** rows of this table, grouping the data bits into dibits, starting with 10 for condition A and 00 for condition B.

Logic Analyzer symbols are hexadecimal values derived from combinations of binary data in selected channels. They should not be confused with the symbols used in M-*aray signaling.*

In this manual, the channel selections for each Logic Analyzer symbol, and the hexadecimal symbol values, are shown in square brackets.

Channels and symbols

The Logic Analyzer display includes a **Clock** channel, eight data channels **Ch 1** to **Ch 8**, each of which displays the sampled binary data (1s and 0s) from one probe, as well as two "symbol" channels **S1** and **S2**. Each of these symbol channels displays a series of hexadecimal numbers that result from combining the binary data from selected data channels.

The data channels that contribute to each symbol channel are selected using the Symbol buttons near the bottom of the screen. By default, all Symbol buttons are up (no channels are selected). Each selected channel contributes one bit to the hexadecimal symbol value; the most significant bit (MSB) corresponding to the leftmost pressed-down button and the least significant bit (LSB) corresponding to the rightmost pressed-down button.

For example, if channels [ch1, ch3, ch6, ch7] are selected for Symbol 1, the hexadecimal values displayed in the S1 channel correspond to $2^3 \times$ Ch 1 + $2^2 \times$ Ch 3 + $2^1 \times$ Ch 6 + $2^0 \times$ Ch 7. In this case, since four data channels are combined into one symbol, the symbol values can range from [0] to [F] (0000_2 to 1111_2). If only two data channels are combined into one symbol, the symbol values can range from [0] to [3] (00_2 to 11_2).

Represent each of the dibits in Table 3 as a hexadecimal value where, if the two digits of the dibit are (b_1, b_0), the hexadecimal value is $2 \times b_1 + b_0$. This will help in interpreting the symbols displayed by the Logic Analyzer.

Table 3. Serial to Parallel Converter inputs and outputs.

Data Bits		1	0	0	1	1	0	0	0	1	1	1	0	1	1	1	0	1
A	**Dibit**	1	0															
	Hex	2																
B	**Dibit**		0	0														
	Hex		0															

Table 3. Serial to Parallel Converter inputs and outputs.

Data Bits		1	0	0	1	1	0	0	0	1	1	1	0	1	1	1	0	1
A	**Dibit**	1	0	0	1	1	0	0	0	1	1	1	0	1	1	1	0	
	Hex	2		1		2		0		3		2		3		2		
B	**Dibit**		0	0	1	1	0	0	0	1	1	1	0	1	1	1	0	1
	Hex		0		3		0		1		3		1		3		1	

13. Connect two more Logic Analyzer probes as follows:

Connect the probes exactly as shown so that the Logic Analyzer will display the symbols as shown in Table 3.

Logic analyzer probe	Connect to	Signal
3	TP6	Serial to Parallel Converter output (MSB)
4	TP7	Serial to Parallel Converter output (LSB)

To make it easier to connect the probes, you may wish to zoom into this region of the diagram. To zoom in a diagram, right-click on the diagram and choose *Zoom* in the context-sensitive menu. This changes the mouse pointer to 🔍. Drag the mouse pointer up or down to zoom in or out. Another way to zoom is to click the diagram and roll the mouse wheel.

14. Record data with the Logic Analyzer and examine the data. Using the Symbol buttons, set Symbol 1 to [ch2] and Symbol 2 to [ch3, ch4].

Examine the data displayed by the Logic Analyzer. Figure 11 and Figure 12 show the two possible conditions, depending on how the Serial to Parallel Converter groups the data sequence into dibits.

Click the Drop 1 Bit button *once only* in the Serial to Parallel Converter and perform another recording. Ch 2 and S1, the input data, will not change but the results in Ch 3, Ch 4 and S2 should be different.

Under each of Figure 11 and Figure 12, identify which of the two possible conditions (A or B) from Table 3 the figure represents.

Because the Serial to Parallel Converter operates on two bits at a time, it introduces a slight delay in the output bit streams. The timing relationship changes slightly after clicking Drop 1 Bit.

Logic Analyzer Settings:
Display Width ..... 10 ms
Source ..... Ch 1
Source Edge ..... Rising
Clock Edge ..... Falling
S1 Data ..... [ch2]
S2 Data ..... [ch3, ch4]

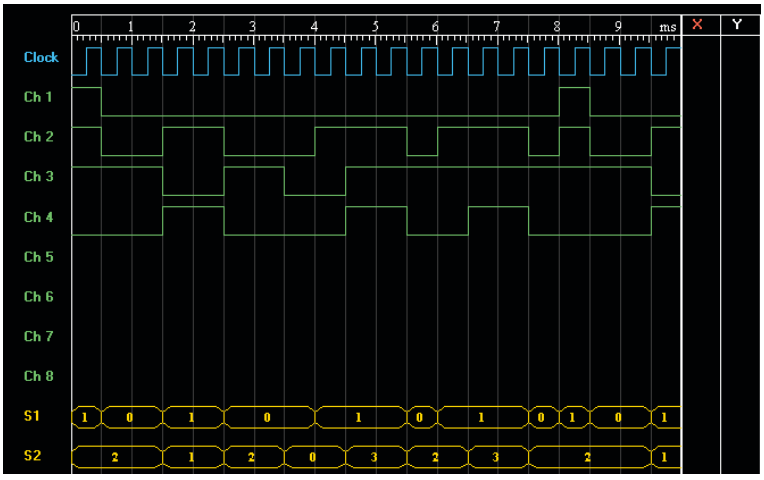


Figure 11. Serial to Parallel Converter input (Ch 2) and outputs (Ch 3 and Ch 4).

Figure 11 represents: ☐ Condition A ☐ Condition B

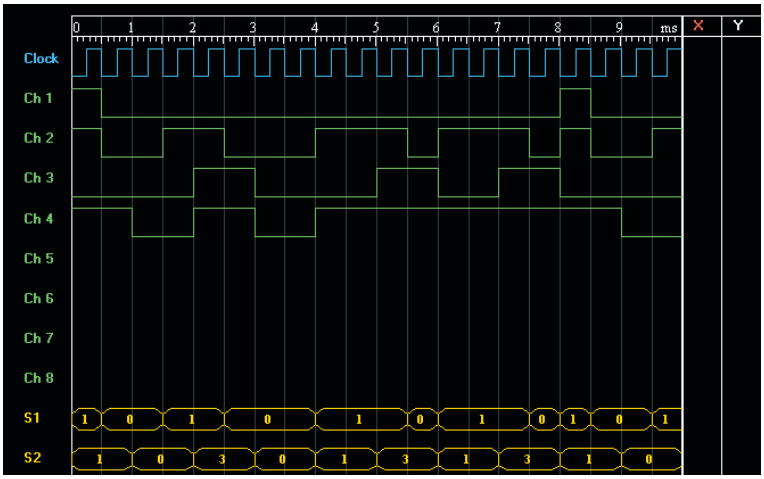


Figure 12. Serial to Parallel Converter input (Ch 2) and outputs (Ch 3 and Ch 4).

Figure 12 represents: ☐ Condition A ☐ Condition B

Oscilloscope Settings:
Display Width..... 10 ms
Source..... Ch 1
Source Edge .....Rising
Clock Edge ..... Falling
S1 Data..... [ch2]
S2 Data..... [ch3, ch4]

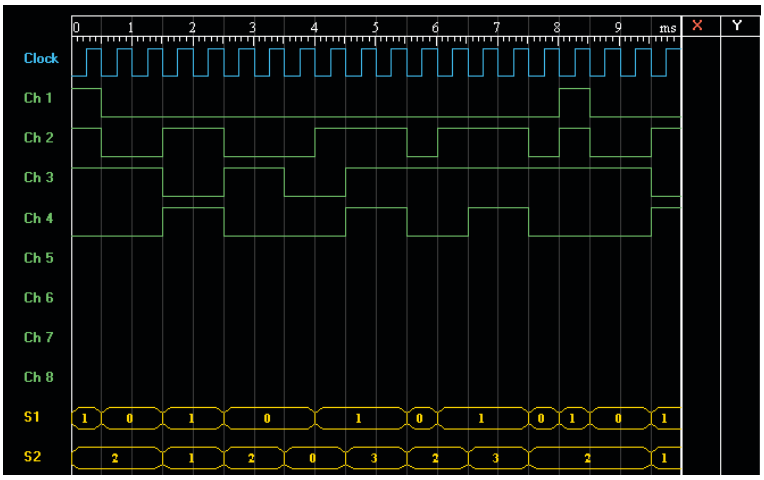


Figure 11. Serial to Parallel Converter input (Ch2) and outputs (Ch3 and Ch4).

Figure 11 represents: ☑ Condition A ☐ Condition B

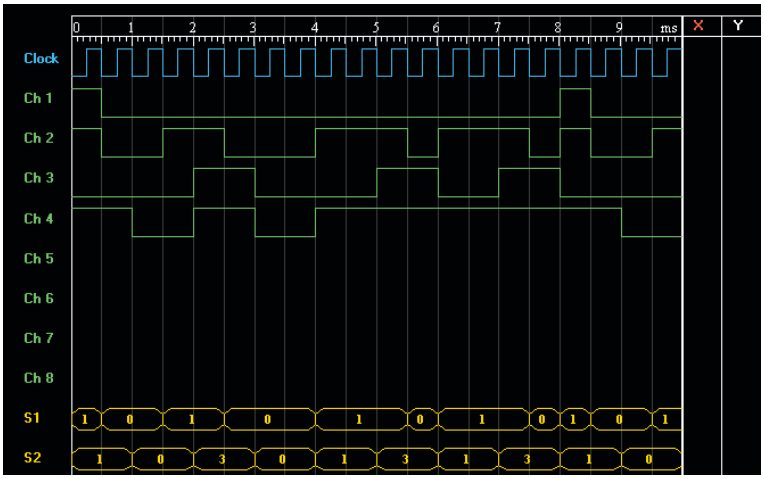


Figure 12. Serial to Parallel Converter input (Ch2) and outputs (Ch3 and Ch4).

Figure 12 represents: ☐ Condition A ☑ Condition B

15. Use the oscilloscope to determine the exact timing relationship of the different signals. Since this requires observing several signals at a time, it will be helpful to use the memory of the Oscilloscope.

Click M1 or M2 in the instrument toolbar to store the current display in Memory 1 or Memory 2. Use the Memories setting to show the contents of Memory 1, Memory 2, or both.

Is the output of the Serial to Parallel Converter triggered by the rising edge or the falling edge of the clock signal? Does this correspond to the symbol used at the clock input of the Serial to Parallel Converter?

The Serial to Parallel Converter output is falling-edge triggered, as indicated by the symbol at the clock input  .

Level Converter

16. Connect the Oscilloscope probes as follows:

Oscilloscope probe	Connect to	Signal
1	TP6	Serial to Parallel Converter output (MSB)
2	TP10	I-channel Level Converter output
E	TP5	Frequency Divider output

To disconnect a probe and return it to the Probes bar, you can right-click the probe and choose *Disconnect Probe* in the context-sensitive menu. Alternatively, you can double-click the probe's place holder in the Probes bar.

The Frequency Divider divides the BSG SYNC. signal frequency in order to generate a signal that can be used as a trigger for the Oscilloscope or the Logic Analyzer. This is necessary when observing the Serial to Parallel Converter output with a binary sequence having an odd number of bits. (All pseudo-random sequences have an odd number of bits.)

Figure 13 shows an example what you may observe.

Generator Settings:
Generation Mode .....Pseudo-Random
n 3
Bit Rate ..... 1500 bit/s

Oscilloscope Settings:
Channel 1.....5 V/div
Channel 2.....2 V/div
Channel E .....5 V/div
Time Base..... 1 ms/div
Trigger: Source .....Ext

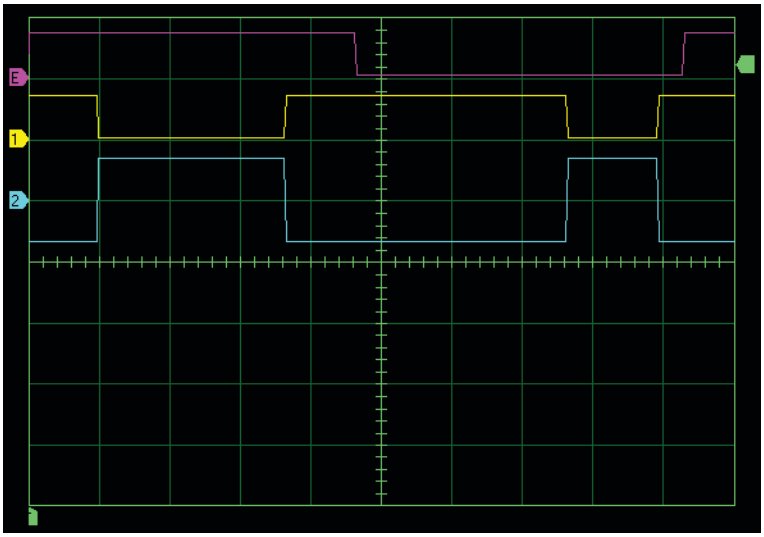


Figure 13. Level Converter input and output signals.

Explain the operation of the Level Converter.

The Level Converter converts the digital data signal into a bipolar analog pulse signal. A digital 0 and a digital 1 at the input of the Level Converter produce an output of approximately +1.34 V and -1.34 V respectively.

The Filters and mixers

17. On the Oscilloscope, store the current waveforms in Memory 1. Then connect the probes as follows.

Oscilloscope probe	Connect to	Signal
1	TP12	I-channel Filter output
2	TP16	I-channel mixer output

Figure 14 shows what you could observe.

QPSK Settings:
Carrier Frequency..... 3000 Hz

Generator Settings:
Generation Mode.....Pseudo-Random
n 3
Bit Rate ..... 1500 bit/s

Oscilloscope Settings:
Channel 1.....2 V/div
Channel 2.....2 V/div
Channel E ..... Off
Time Base..... 1 ms/div
Trigger: Source .....Ext
Memories .....Memory 1

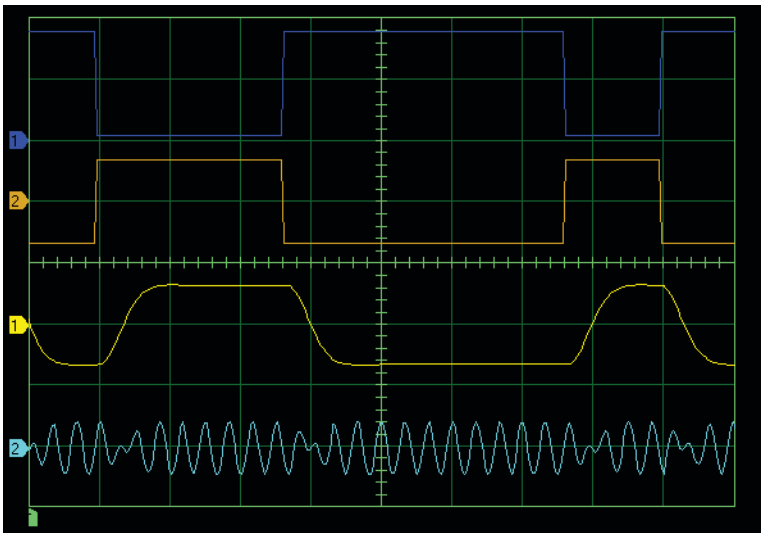


Figure 14. Level Converter and mixer inputs (Ch 1) and outputs (Ch 2).

What is the effect of the filter on the bipolar data signal and on the mixer output signal? What is the advantage of filtering the data signal before modulation?

The low-pass filter smoothes the transitions in the analog data signal. Since rapid changes lead to undesirable frequency components in the modulated signal, filtering reduces the bandwidth of the QPSK signal. (It also introduces amplitude variations in the mixer output signal accompanying each phase change.)

18. Using a PRBS as input data to the modulator, use the Spectrum Analyzer to compare the spectra of the following signals (see Figure 15):

- The DATA INPUT signal (TP1)
- The data signal at the MSB output of the Serial to Parallel Converter (TP6)
- The bipolar data in the I-channel (TP12) with the Low-Pass Filters both On and Off.

a. What is the frequency spacing of the nulls in the Input Data spectrum. What does this correspond to?

The nulls in the DATA INPUT spectrum are spaced at intervals equal to the bit rate.

b. What is the frequency spacing of the nulls in the spectrum of the Serial to Parallel output. Explain.

The nulls in the Serial to Parallel Converter I-channel data are spaced at one-half the input data bit rate (that is, at the symbol rate). This is because the bit rate at each of the Serial to Parallel Converter outputs is one half the input data bit rate.

c. What effect have the Level Converter and the low-pass Filter on the signal spectrum?

The Level Converter has no effect on the frequency spectrum of the signal. The Filter attenuates the high-frequency components of the signal.

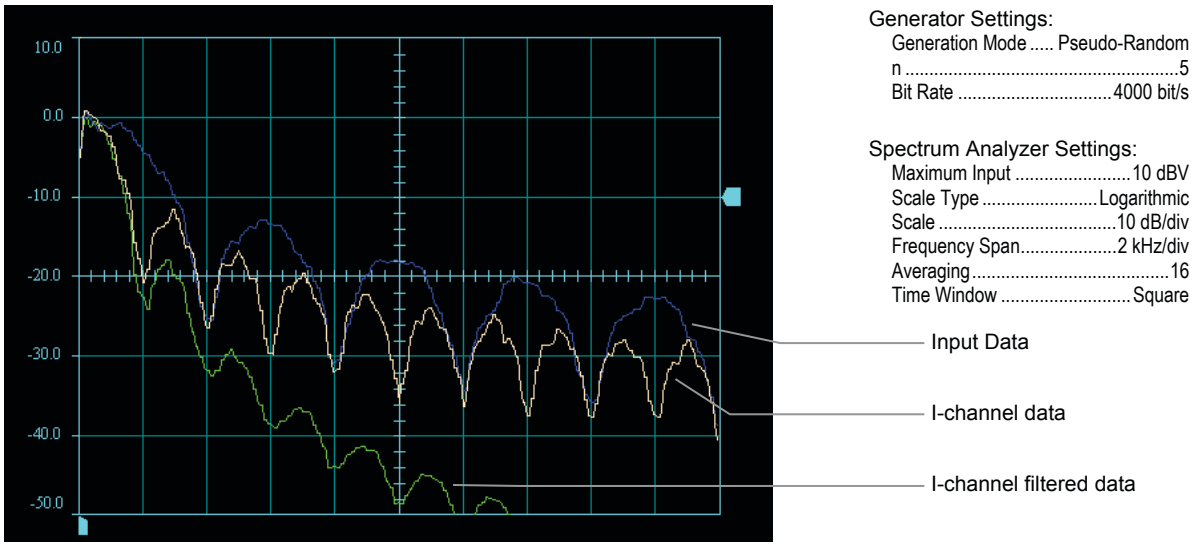


Figure 15. Spectra of input data and I-channel bipolar data.

19. Connect Oscilloscope probe E to TP13 (the I-channel carrier signal). Turn the Low-Pass Filters Off and observe the signals using settings that allow you to see detail. Then turn the Low-Pass Filters On (see Figure 16 and Figure 17).

QPSK Settings:
Carrier Frequency..... 2000 Hz

Generator Settings:
Generation Mode .....Pseudo-Random
n 3
Bit Rate ..... 1500 bit/s

Oscilloscope Settings:
Channel 1.....2 V/div
Channel 2.....2 V/div
Channel E .....2 V/div
Time Base..... 1 ms/div
Trigger: Source .....Ext

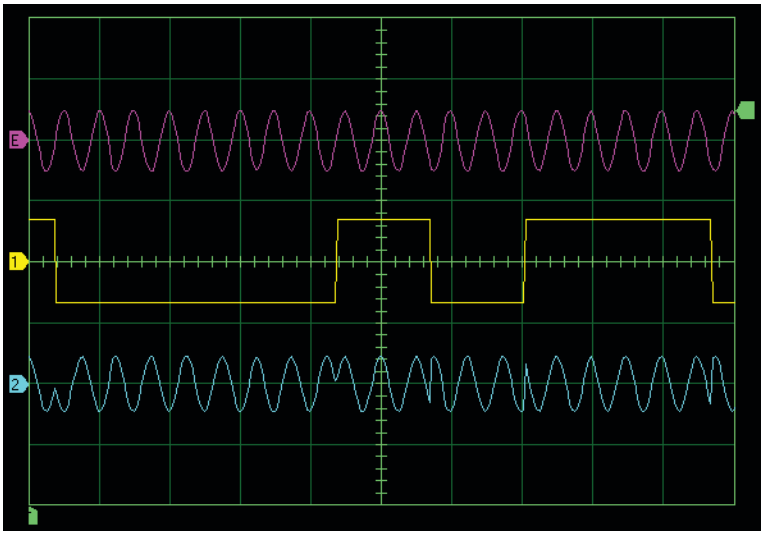


Figure 16. I-channel carrier, bipolar data and BPSK signal (Low-Pass Filters Off).

Oscilloscope Settings:
Channel 1.....2 V/div
Channel 2.....2 V/div
Channel E .....2 V/div
Time Base..... 1 ms/div
Trigger: Source .....Ext

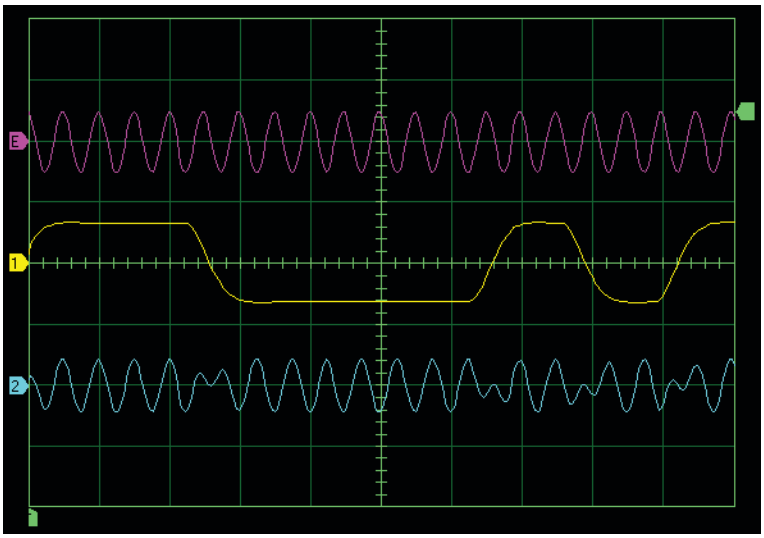


Figure 17. I-channel carrier, bipolar data and BPSK signal (Low-Pass Filters On).

Describe how the phase of the BPSK signal changes when the filters are Off and when they are On.

With the filters Off, the change in phase is abrupt, causing discontinuities in the BPSK signal. When the filters are On, the phase change is gradual. The amplitude decreases to near zero and then increases with the new phase.

20. Use the oscilloscope to observe the I- and Q-channel carrier signals. How are these signals related?

The I- and Q-channel carrier signals are in quadrature (out of phase by 90°). If the I-channel carrier is considered to be a cosine wave, the Q-channel carrier corresponds to a sine wave.

21. Observe the operation of the mixers in both the I and Q channels using different Carrier Frequency values.

The summer

22. Use the Oscilloscope to observe the signals at the input and output of the summer (TP16, TP17, and TP18). Figure 18 shows an example.

As an option, use a conventional oscilloscope to observe the signal at the QPSK Modulator OUTPUT (refer to the RTM Connections tab of the software).

QPSK Settings:
Carrier Frequency..... 10000 Hz
Low-Pass Filters ..... Off

Oscilloscope Settings:
Channel 1.....1 V/div
Channel 2.....1 V/div
Channel E .....1 V/div
Time Base.....50 µs/div
Trigger: Source ..... Ch 1

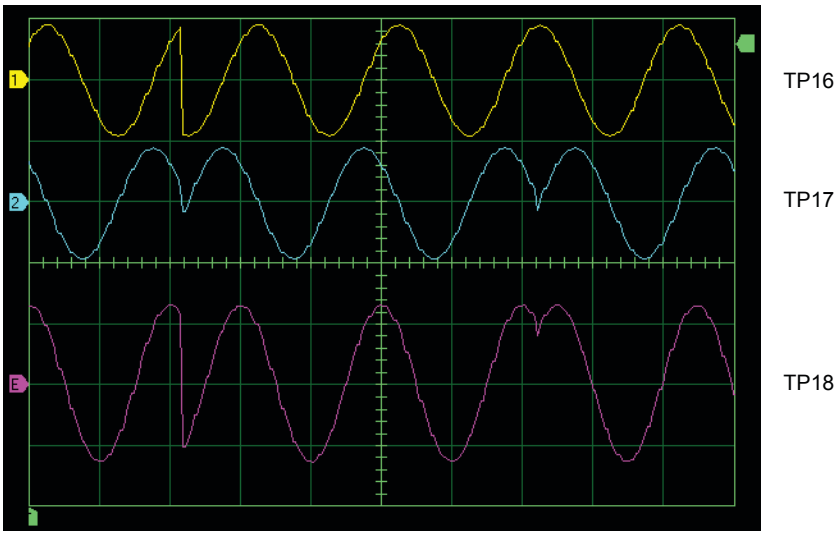


Figure 18. Summer input (BPSK) and output (QPSK) signals.

Describe the operation of the summer.

The summer sums the I-channel and Q-channel BPSK signals to produce the QPSK signal.

23. Use the Spectrum Analyzer to observe the spectrum of the QPSK signal and compare this with the spectrum of the I-channel BPSK signal.

Express the bandwidth of the QPSK signal in terms of the bit rate and the symbol rate.

The nulls in the QPSK signal spectrum occur at multiples of the symbol rate R_s which is one-half the bit rate R_b. The first-nulls bandwidth of the QPSK signal is therefore $2R_s = R_b$.

Compare the bandwidths and bit rates of the I-channel BPSK signal and the QPSK signal. Explain why QPSK is considered to be a bandwidth efficient modulation technique.

The Spectrum Analyzer shows that the first nulls bandwidth of the I-channel BPSK signal and the QPSK signal are the same. The bit rate of the I-channel BPSK signal is $R_b/2$ (one-half the total bit rate of the modulator) whereas the bit rate of the QPSK signal is R_b. QPSK is bandwidth efficient because it can transmit data at twice the bit rate over the same bandwidth as binary modulation techniques such as BPSK.

Signal constellations

24. Connect the Oscilloscope probes as follows:

Oscilloscope probe	Connect to	Signal
1	TP10	I-channel Level Converter output
2	TP11	Q-channel Level Converter output

The Logic Analyzer probes should be connected as follows:

Logic analyzer probe	Connect to	Signal
C	TP2	CLOCK INPUT
2	TP1	DATA INPUT
1	TP3	BSG SYNC. OUTPUT
3	TP6	Serial to Parallel output (MSB)
4	TP7	Serial to Parallel output (LSB)

Make the following Binary Sequence Generator settings:

Generation Mode ..... Pseudo-Random
n 3
Bit Rate ..... 2000 bit/s

Use the Oscilloscope in the X-Y mode to observe the constellation, as shown in Figure 19.

As an option, connect a conventional oscilloscope to the QPSK Demodulator I-CHANNEL OUTPUT and QPSK Demodulator Q-CHANNEL OUTPUT (refer to the RTM Connections tab of the software). Use the conventional oscilloscope in the X-Y mode to observe the constellation. (The Low-Pass filters in the QPSK Modulator must be set to On.)

Oscilloscope Settings:
Channel 1.....1 V/div
Channel 2.....1 V/div
Display Mode..... Dots
X-Y.....On
Sampling Window.....50 ms

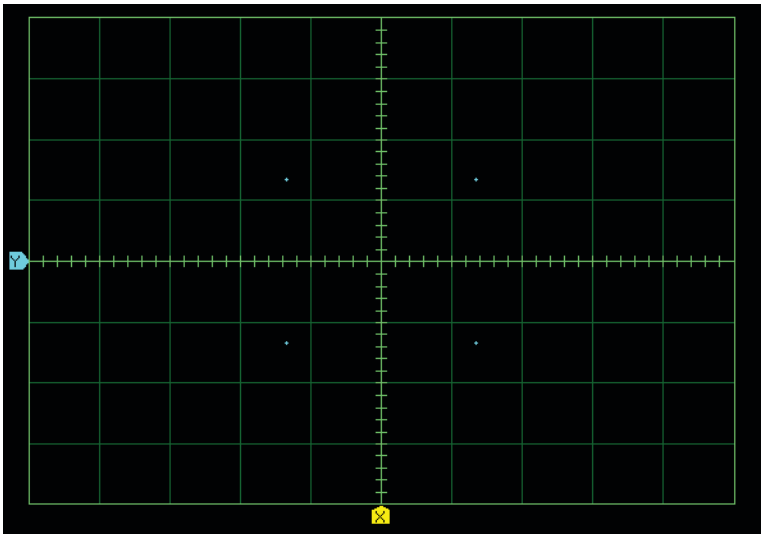


Figure 19. QPSK constellation.

What information does this constellation provide?

The signal constellation shows all possible signal states (symbols). In the case of QPSK, it shows that there are four equally-spaced phases available and that each signal state has the same amplitude.

25. Set the Generation Mode to User-Entry. Set the Binary Sequence to each of the following two-bit sequences (dibits): 00 and 11. For each sequence, record data using the Logic Analyzer and note which dibit is present at the outputs of the Serial to Parallel Converter (see Figure 20).

Display Width.....10 ms
Source.....Ch 1
Source Edge.....Rising
Clock Edge.....Falling
S1 Data.....[ch3]
S2 Data.....[ch4]

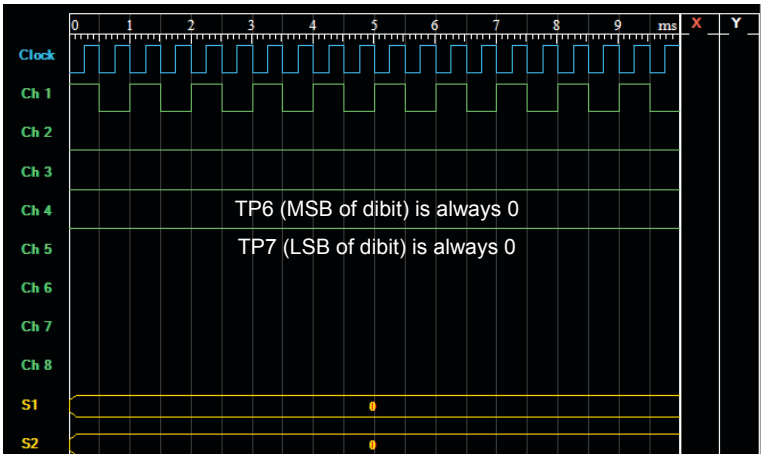


Figure 20. Logic Analyzer showing the dibit 00 at TP6-TP7.

Observe the Oscilloscope display, for each sequence. Write in the boxes in Figure 21 the dibits that corresponds to these two constellation points.

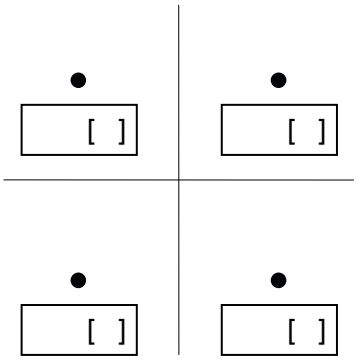


Figure 21. Dibits in the QPSK constellation.

Set the Binary Sequence to 01. Record data on the Logic Analyzer and note which dibit is present at the outputs of the Serial to Parallel Converter. Since TP6 represents the MSB, a 1 at TP6 and a 0 at TP7 represents the dibit 10. Clicking the Drop 1 Bit button will change this dibit to 01.

Click the Drop 1 Bit button several times, each time observing the dibit using the Logic Analyzer and observing the display on the Oscilloscope. Then write in the boxes in Figure 21 the dibits that corresponds to two missing constellation points. Then write the hexadecimal value for each dibit in the square brackets.

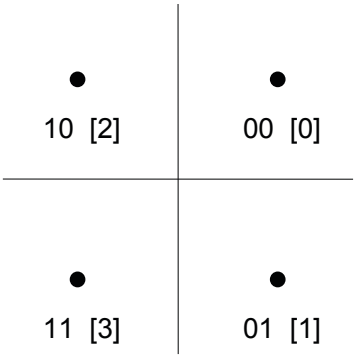


Figure 21. Dibits in the QPSK constellation.

26. Enter the Binary Sequence 1100 and observe the constellation. Click the Drop 1 Bit button and explain what you observe.

Since the Serial to Parallel Converter is not synchronized with the input data stream, this binary sequence may be interpreted as 11001100… or 10011001…. In the first case, only the dibits 11 and 00 are sent to the modulator and only these two points appear in the constellation. In the second, only the dibits 10 and 01 are sent. Clicking the Drop 1 Bit button switches between these two conditions.

27. Enter the Binary Sequence 101. Why does this 3-bit sequence produce three constellation points, each of which represents two bits?

This sequence has an odd number of bits. Since the Serial to Parallel Converter groups bits two at a time, the sequence must pass twice before the system returns to its initial state. The dibits sequence sent to the modulator is therefore 10 11 01… These three points appear in the constellation.

28. Experiment with various Binary Sequences and observe the results on the Oscilloscope.

29. When you have finished using the system, exit the LVCT software and turn off the equipment.

Conclusion

In this exercise, you became familiar with the LVCT software and studied the operation of the basic functional blocks of the QPSK modulator. You observed that the Serial to Parallel Converter groups the input data stream into dibits that are processed by two parallel channels, I and Q, and that the starting point of this grouping is arbitrary. You saw how the Level Converters and the mixers generate two BPSK signals using two carriers in phase quadrature. You observed that summing the two BPSK signals produces the QPSK signal. Observing the spectrum of the QPSK signal showed that QPSK is more bandwidth-efficient than binary modulation techniques. You also observed the signal constellation on the oscilloscope for various binary sequences.

Review Questions

1. Explain what is meant by bandwidth efficiency.

Bandwidth efficiency is a measure of how efficiently a modulation technique uses the available bandwidth. It is equal to the maximum theoretical number of bits per second that can be transmitted per Hz of bandwidth.

2. How does the bandwidth efficiency of QPSK compare to that of binary modulation techniques?

The bandwidth efficiency of QPSK is twice that of binary modulation techniques.

3. What does a constellation diagram represent?

The constellation diagram is a pictorial representation showing all possible signal states as a set of constellation points in the I-Q plane. Each constellation point corresponds to the head of a phasor and represents one of the symbols used by the modulation scheme. Its position in the diagram shows the amplitude and the phase of the corresponding waveform.

4. What is the role of the mixers in the QPSK modulator?

Each mixer performs modulation by multiplying the sinusoidal carrier by the bipolar data signal in order to produce a BPSK signal. The effect of the mixer is to shift the frequency spectrum of the baseband signal up to the frequency of the carrier.

5. How are the signals at the outputs of the mixers combined to produce the QPSK signal?

The I- and Q-channel BPSK signals are simply summed in order to produce the QPSK signal.

Bibliography

STREMLER, Ferrel G., *Introduction to Communications Systems*, Second Edition, Reading, Mass., Addison-Wesley, 1982.
ISBN 0-201-07251-3

SKLAR, Bernard. *Digital Communications Fundamentals and Applications*, Second Edition, Upper Saddle River, N.J., Prentice Hall Inc., 2001
ISBN 978-0-13084-788-7